PROCESS EVALUATION AND OPTIMIZATION FOR EUV MANUFACTURING

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Abstract

In the first half of 2011, the ASML NXE:3100 pre-production scanner was installed at imec. The NXE:3100 is equipped with a laser-assisted discharge produced plasma source from XTREME technologies, and is interfaced to a TEL CLEAN TRACK™ LITHIUS Pro™ -EUV.
We discuss the performance and optimization of the resist processes on the NXE:3100 cluster. After meeting preliminary resist screening criteria, gallon bottle samples of different resist platforms are installed on the EUV cluster for detailed benchmarking and optimization. The work focuses on optimization of across wafer critical dimension uniformity and process defect levels. The TEL smoothing process is optimized and manufacturability is greatly improved.

Process evaluation conditions

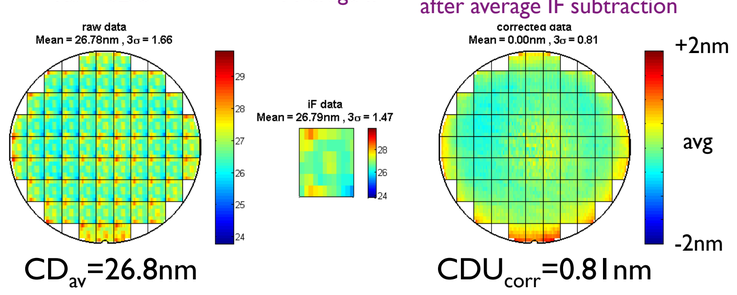
Processes evaluated:
Resist A on UL (20nm): 3100 qualification process
Resist B on UL (20nm), FIRM™Extreme™: new process of record
Resist C on UL (20nm), FIRM™Extreme™: new POR candidate

Evaluation tests:
CDU27: 27nm LS, conventional illumination, 50nm resist FT
CDU22: 22nm LS, dipole 60x illumination, 40nm resist FT
CH-CDU30: 30nm CH (20%bias), conventional ill., 60nm resist FT
DEF32: 32nm LS, conventional illumination, 50nm resist FT
Line roughness: 27nm LS (cfr. CDU27 wafers)

CDU27

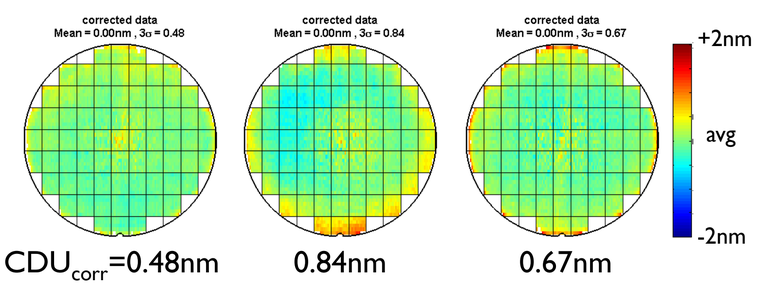
Qualification and monitoring target structure of NXE:3100.

Baseline process conditions: resist A, LD puddle, TMAH, DIW rinse
Process evaluation based on IF corrected CDU from YS scatterometry.



CD_{av}=26.8nm
CDU_{corr}=0.81nm

DEV process evaluation

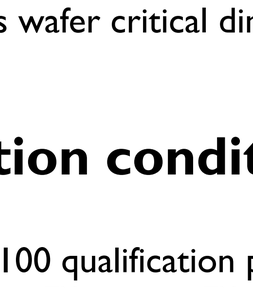


CDU_{corr}=0.48nm
0.84nm
0.67nm

For 27nm LS, resist A and B perform equally well. MGP allows more tuning of the process, resulting in superior CDU performance.

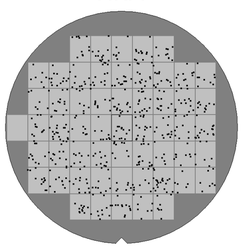
DEF32

Baseline process conditions:
Resist A, LD puddle,
TMAH, DIW rinse
Defect inspection on
KLA2835.



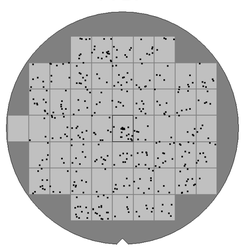
492 defects
Density = 1.41 defects/cm²

FIRM™

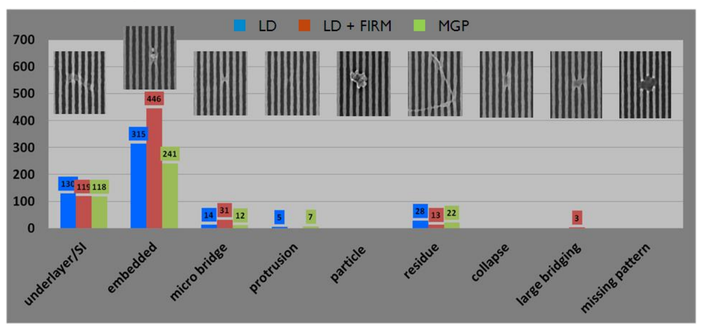


612 defects
Density = 1.76 defects/cm²

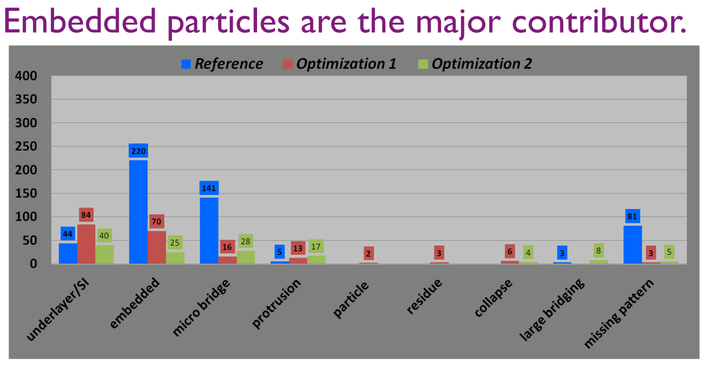
MGP



400 defects
Density = 1.15 defects/cm²



Embedded particles are the major contributor.

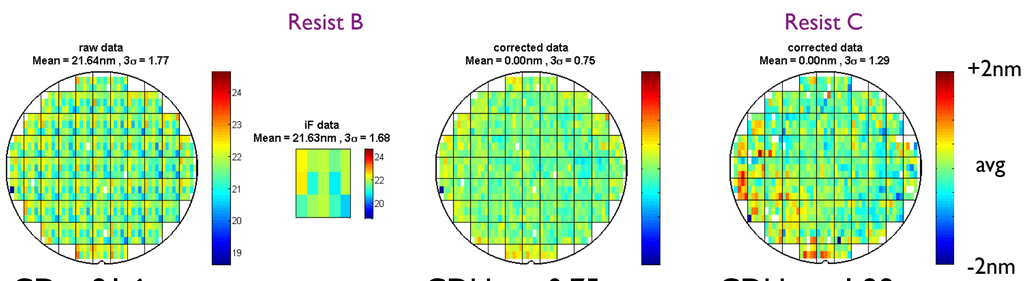


After several optimizations, the defect density is reduced to 0.36defects/cm².

CDU22

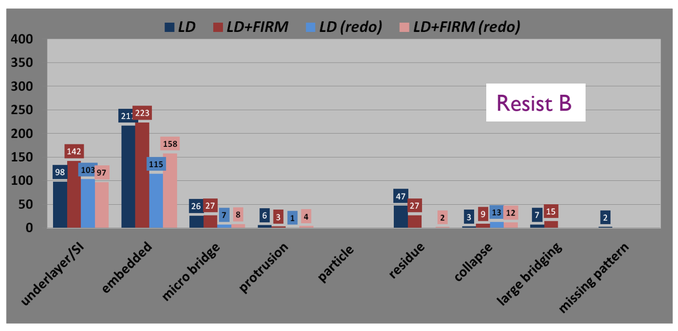
Qualification target structure of NXE:3300.

Process conditions: resist B, LD puddle, TMAH, FIRM™ rinse
Process evaluation based on IF corrected CDU from CD-SEM.

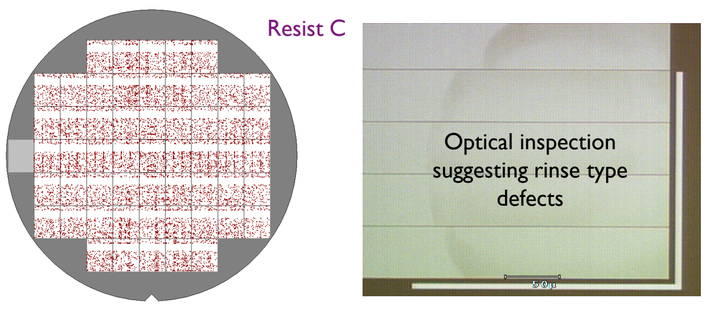


CD_{av}=21.6nm
CDU_{corr}=0.75nm
CDU_{corr}=1.29nm

Both resist B and C can be used to print 22nm LS. CDU performance of resist B is better.

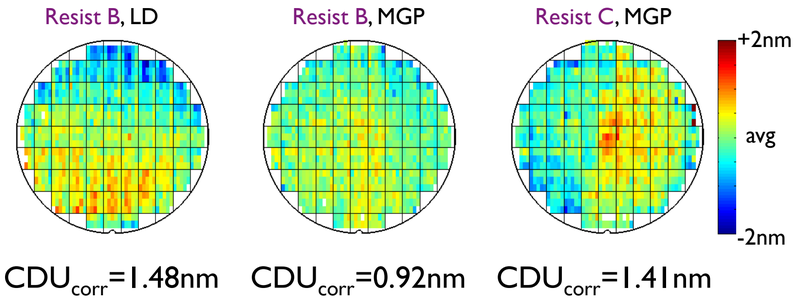


Resist B shows similar performance, improving when more wafers are run. FIRM™ hardly impacts defectivity.



Different routes are followed to improve the process, some of them look promising. Optimization still ongoing.

CH-CDU30

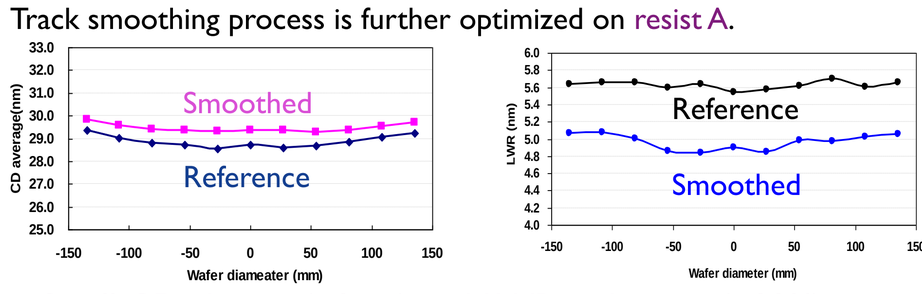


CDU_{corr}=1.48nm
CDU_{corr}=0.92nm
CDU_{corr}=1.41nm

Also for contact holes, MGP and resist B give lowest CDU.

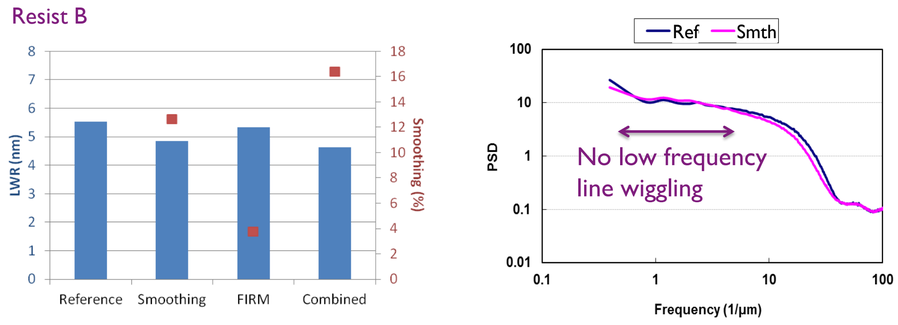
Line roughness

Track smoothing process is further optimized on resist A.



Small CD change (<1nm) and LWR reduction (~11%) is uniform over the wafer.

Resist B



Smoothing and FIRM™ have additive effect giving 16.5% total LWR reduction without degrading the lines.

Conclusion

Overall process contribution to CDU is small (<1nm after optimization).
Dedicated process improvements bring defect density down to 0.4defects/cm², and route to further reduction is identified.
New resist C shows some particular process challenges.
Smoothing process now optimized for 2 resists with good uniformity and maintaining line integrity.

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